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| 10/719,192 | 11/21/2003 | Seung-Kwon Baek | 5649-1185 | 2998 |

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| EXAMINER | |
|---|---|
| MALEK, LEILA | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/719,192 | BAEK ET AL. | |
| | Examiner | Art Unit | |
| | LEILA MALEK | 2611 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *11 November 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *8,12 and 21-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8,12,21-28 and 30-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 May 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Amendment*

1. This office action is in response to the amendments received on 11/11/2009.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 8, 12, 23-25, 27, 28, and 30-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan (US 7,065,036), in view of Perry (US 3,988,601).

As to claim 8, Ryan discloses a method of transforming an OFDM signal (see Fig. 4) by a FFT processor (see Fig.5, block 511 and column 9, lines 28-30), the OFDM signal having a symbol (see Fig. 4), the symbol including a preamble, and first data following the preamble, the preamble having a sequence of N-samples (i.e. because of the ADC 301 in Fig. 5), the method comprising: storing the preamble in a memory as the OFDM signal is received (see Fig. 5, block 507); reading the preamble from the memory (see column 9, lines 5-12); transforming the preamble by a fast Fourier transform into a transformed preamble (see block 511 and column 9, lines 28-32). Ryan does not discloses reading the preamble in response to an end point of the preamble being

detected, however, in view of lack of any explanation by the Applicant on why reading the preamble does not occur until the end point of preamble has been detected, Examiner states that the time of reading from the memory is a matter of design choice and it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ryan and does not start the reading until the end point of the preamble has been detected to meet the design requirements of the system. Ryan also does not disclose storing the transformed preamble in the memory. However, it would have been obvious to one of ordinary skill in the art at the time of invention to save the output of the FFT in a memory (or a similar device) for further processing. Moreover, Ryan does not disclose that the data sequence has N/2 samples. However, the size of the data symbols is a matter of design choice and it would have been obvious to one of ordinary skill in the art to choose the size of the data symbols half the size of the preamble to meet the design requirements of the system. Ryan discloses buffering (see blocks 507 and 510) the first data that follows the preamble and transforming a first data and a second data (see Fig. 4 DATA1 and DATA2) that is received by the FFT processor (see block 511) using a FFT transform and outputting a data signal (see column 9, lines 28-32). Ryan further discloses buffering first data that follows the preamble while the preamble is transformed (see column 9, lines 5-33). Ryan discloses all the subject matters claimed in claim 1, except for simultaneously transforming second data that is received by the FFT processor after the first data is buffered and that has a sequence of N/2 samples, and the buffered first data, respectively, using an N-point FFT transform into third data as

the second data is received, and storing the third data in the memory, and outputting the third data. Perry discloses a method for transforming an incoming data signal. Perry discloses splitting the received data to two parallel branches (see Fig. 1). Buffering the data travelling on the first branch (i.e., the first data), simultaneously transforming second data (i.e., the data traveling on the branch with no buffer) that is received by the FFT processor (see Fig. 11) after the first data is buffered (see block 12) and that has a sequence of N/2 samples (see column 1, last paragraph), and the buffered first data, respectively, using an N-point FFT transform (the number of inputs of the FFT block should be the same as the number of samples, therefore in this case is N/2+N/2, (N/2 is the number of samples received from each branch) into third data as the second data is received (see the output of the FFT block 11), and storing the third data in the memory (see block 15), and outputting the third data (see the output of block 15). It would have been obvious to one of ordinary skill in the art to modify Ryan and process the data portion of the OFDM frame as taught by Perry to reduce the size and cost of the FFT buffer.

As to claim 12, Perry discloses that the first data travelling through the register is delayed by an amount equal to the size of the first data, because Perry discloses that when the first sample reaches the FFT processor from the register 12, the (s+1)th sample is available at the other input of the FFT processor (see column 2, lines 13-15). Therefore, it means that the amount of the delay on the first signal is equal to the size of the first data. As explained above, in the rejection of claim 8, the size of the first data can be N/2.

As to claim 23, Perry shows transforming the first data and the second data into third data comprises supplying the first data from an input buffer to a first input of an FFT processing element and supplying the second data directly (see Fig. 1, blocks 12 and 11) from an analog to digital converter (see column 1, last paragraph, where Perry discloses that the received signal is the sampled signal therefore it inherently comes from an ADC) to a second input of an FFT processing element without buffering the second data.

As to claim 24, Ryan discloses that the first data and the second data are provided to the FFT processing element in response to completion of the step of transforming the first long preamble and the second long preamble (see column 9, lines 14-33, wherein Ryan discloses that first the preamble has been processed by the FFT (see lines 14-27) and then the rest of the data has been processed in natural time order).

As to claim 25, Ryan discloses transforming the first and second preambles (see Fig. 4, first and second LS; and column9, lines 28-32). However, neither Ryan nor Perry discloses forming an average of the first preamble and the second preamble, wherein transforming the preamble comprises transforming the average of the first preamble and the second preamble. In view of further explanation on why an average of the preambles has been used instead of the preambles, Examiner states that using an average of the preambles is a matter of design choice and it would have been obvious to one of ordinary skill in the art at the time of invention to transform the average of the preambles to meet the design requirements of the system.

As to claim 27, Ryan discloses finishing the fast Fourier transform method when the symbol is a final symbol, and continuing the FFT processing when the symbol is not the final symbol (see column 9, lines 28-32, where Ryan discloses that the whole data has been transformed by FFT unit).

As to claim 28, Ryan discloses a Fast Fourier Transform (FFT) processor (see Fig. 5, block 511) for demodulating an orthogonal frequency division multiplexing (OFDM) signal (see Fig. 4) including a preamble having a sequence of N samples (see the output of the ADC 301 in Fig. 5) and first data following the preamble (see Fig. 4), the FFT processor comprising: a timing acquisition section that is configured to output a timing signal in response to detecting an end point of the preamble (see column 5, lines 55-56, Ryan does not disclose that the SOP detects the end of the preamble, however, detecting the start of data is the same as detecting the end of the preamble); a controller (see block 535) that is configured to output a first control signal and a second control signal in response to the timing signal (see the SOP_boundary signal); a signal converter (see blocks 507, 510, and 511) that is configured to store the preamble in response to the first control signal (see the output of 535 that controls FIFO and other units and column 9, lines 14-27), to transform the preamble by an N-point FFT into a second preamble (see block 511); and an FFT input buffer (see block 510) that is configured to store the samples of the first data while the preamble is being transformed (see column 9, lines 14-33, wherein Ryan discloses that the first samples to be transformed are the preamble samples and then the other samples have been transformed in natural time order). Ryan does not disclose

that the data has a sequence of N/2 samples. However, size of the data block (i.e. the number of samples in the data block) is a matter of design choice and it would have been obvious to one of ordinary skill in the art at the time of invention to use a data sequence having N/2 samples to meet the design requirements of the system. Ryan also does not disclose saving the transformed preamble. However, it would have been obvious to one of ordinary skill in the art at the time of invention to save the transformed preamble to make the preamble accessible for processing. Ryan discloses all the subject matters claimed in claim 28, except that the signal converter is further configured to perform an N-point FFT of the buffered first data and second data as the second data is sequentially received to transform the first data and the second data into third data having N samples. Perry discloses a method for transforming an incoming data signal. Perry discloses splitting the received data to two parallel branches (see Fig. 1). Buffering the data travelling on the first branch (i.e., the first data), simultaneously transforming second data (i.e., the data traveling on the branch with no buffer) that is received by the FFT processor (see Fig. 11) after the first data is buffered (see block 12) and that has a sequence of N/2 samples (see column 1, last paragraph), and the buffered first data, respectively, using an N-point FFT transform (the number of input of the FFT block should be the same as the number of samples, therefore in this case is N/2+N/2) into third data as the second data is received (see the output of the FFT block 11), and storing the third data in the memory (see block 15), and outputting the third data (see the output of block 15). It would have been obvious to one of ordinary skill in the art

to modify Ryan and process the data portion of the OFDM frame as taught by Perry to reduce the size and cost of the FFT buffer.

As to claim 30, Ryan further discloses an analog to digital converter (ADC) (see Fig. 5, ADC 301), wherein the FFT buffer (see block 510) is coupled to the ADC and receives the first data from the ADC and wherein the signal converter (see blocks 507 and 511) is coupled to the ADC. As explained above, Perry shows receiving the first data as buffered data from the FFT input buffer and receives the second data as un-buffered data from the ADC.

As to claim 31, Perry discloses that the first data travelling through the register is delayed by an amount equal to the size of the first data, because Perry discloses that when the first sample reaches the FFT processor from the register 12, the (s+1)th sample is available at the other input of the FFT processor (see column 2, lines 13-15). Therefore, it means that the amount of the delay on the first signal is equal to the size of the first data. As explained above, in the rejection of claim 28, the size of the first data can be N/2.

As to claim 32, Perry discloses that signal converter comprises an FFT processing element (see Fig. 1, block 11) including a first input line configured to receive a sample of the first data and a second input line configured to receive a sample of the second data.

As to claim 33, Ryan discloses a quadrature detector that is configured to receive the OFDM signal, to convert the OFDM signal into a baseband OFDM signal, to generate a real component of the OFDM signal and an imaginary component of the OFDM signal, and to output the real component of the OFDM

signal and the imaginary component of the OFDM signal to the ADC (see column 5, lines 1-20).

3. Claims 21, 22, 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ryan and Perry, further in view of Makoto (see reference #2, cited by the Applicant in IDS submitted on 04/22/2009).

As to claim 21, Ryan and Perry do not disclose that the memory comprises first, second, third and fourth memories, wherein transforming the first data and the second data comprises: activating a first toggle signal that is configured to control read and write operations with respect to the memory when the preamble is transformed by the fast Fourier transform; determining whether or not the first data are transformed by the last Fourier transform the first toggle signal is in an active state: storing in sequence the third data in the first memory and the third memory when the first and second data are transformed by the fast Fourier transform, and outputting in sequence data stored in the second and fourth memories while the third data are stored in the first and third memories; and inverting the first toggle signal, and activating a second toggle signal for controlling the read and write operations with respect to the memories. Makoto, discloses a fast Fourier transform device (see page, paragraph 0006, conventional example 3), comprising a 1$^{st}$ memory, 2$^{nd}$ memory, 1$^{st}$ input buffer, and 2$^{nd}$ input buffer. Makoto further discloses that the data can be divided to a first half (can be considered as preambles) and a second half (can be considered as data information), so that one data may be written in at the same time it reads one data for memories. Makoto discloses that in this example the system begins

to read one data at a time from the 1st and 2nd input buffers, and it inputs into a butterfly computing unit (i.e. the FFT), and it writes at a time two data which is an operation result from this computing unit (interpreted as determining whether or not the first data and the second data are transformed), in the 1st and 2nd memories, begin to read at a time one data which performs a butterfly operation again from the 1st and 2nd memories, and operation of inputting into butterfly computing unit is repeated. Makoto discloses that as the system writes at a time one data which it outputs two pieces at a time as a result of a final butterfly operation in the 1st and 2nd output buffers, improvement in the speed is attained. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ryan and Perry as suggested by Makoto to increase the processing speed of the system. Makoto does not expressly disclose activating a first and second toggle signals to control read and write operations, however, it would have been obvious to one of ordinary skill in the art at the time of invention to use different toggle signals each time (the first time is when the transformed data is saved in the 1st and 2nd memories for the first time, and the second time is when the whole process has been repeated again), to convey the control orders to the memories and synchronize the operation of the memories.

As to claim 22, Makoto does not expressly disclose that the first toggle signal controls the read operation with respect to the first and third memories and controls the write operation with respect to the second and fourth memories, and the second toggle signal controls the write operation with respect to the first and third memories and controls the read operation with respect to the second and

fourth memory. However, setting the first and second toggle signals to perform the above operations is a matter of design choice and it would have been obvious to one of ordinary skill in the art at the time of invention to modify Makoto to read the data from the first and third memories the first time the operation has been performed and to read the data from the second and forth memory the second time the operation has been performed (i.e. during iterations) to meet the design requirements of the system.

As to claim 26, neither Ryan nor Perry discloses that the memory comprises first, second, third and fourth memories each of which is configured to store N/2 samples, wherein storing the third data comprises storing the third data in the first and third memories. However, since smaller memories are cheaper, it would have been obvious to one of ordinary skill in the art at the time of invention to use a plurality of smaller memories instead of one big memory to reduce the cost of the system. Furthermore, the order of saving the data in the memories is a matter of design choice and it would have been obvious to one of ordinary skill in the art at the time of invention to store the transformed data in the first and third memories to meet the design requirements of the system. Perry discloses transforming the entire signal (see column 1, last paragraph and column 2, first and second paragraphs), therefore inherently teaches transforming fourth and fifth data (as explained before can optionally have respective sequences of N/2 samples) into sixth data (see the output of FFT 11); storing the sixth data in the memory (again as explained above there can be optionally more than one memory). Ryan and Perry do not disclose outputting the third data from the first

and third memories while the sixth data is stored. Makoto, discloses a fast Fourier transform device (see paragraph 0006, conventional example 3), comprising a 1st memory, 2nd memory, 1st input buffer, and 2nd input buffer. Makoto further discloses that the data can be divided to a first half (can be considered as preambles) and a second half (can be considered as data information), so that one data may be written in at the same time it reads one data for memories. Makoto discloses that in this example the system begins to read one data at a time from the 1st and 2nd input buffers, and it inputs into a butterfly computing unit (i.e. the FFT), and it writes at a time two data which is an operation result from this computing unit (interpreted as determining whether or not the first data and the second data are transformed), in the 1st and 2nd memories, begin to read at a time one data which performs a butterfly operation again from the 1st and 2nd memories, and operation of inputting into butterfly computing unit is repeated. Makoto discloses that as the system writes at a time one data which it outputs two pieces at a time as a result of a final butterfly operation in the 1st and 2nd output buffers, improvement in the speed is attained. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to modify Ryan and Perry as suggested by Makoto to increase the processing speed of the system.

***Allowable Subject Matter***

4. Claim 29 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEILA MALEK whose telephone number is (571)272-8731. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leila Malek
Examiner
Art Unit 2611

/L. M./
/Leila Malek/
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